

CLMPTO
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CLAIMS 1-8. (CANCELLED)

9. A method for fabricating a semiconductor device, the method comprising:
- (a) forming gate stacks comprising a gate dielectric layer, a gate conductive layer, a capping layer, and a gate spacer, and source and drain regions on a semiconductor substrate;
 - (b) covering a first oxide layer filling spaces between the gate stacks and planarizing the first oxide layer;
 - (c) forming first cell pads connected to the source regions and second cell pads connected to the drain regions in the first oxide layer;
 - (d) forming a second oxide layer on the first oxide layer and the first and second cell pads;
 - (e) sequentially stacking an etch stopper and a third oxide layer on the second oxide layer;
 - (f) forming oxide layer patterns to form damascene bit lines parallel to each other on the second oxide layer by etching the third oxide layer so that each of the oxide layer patterns has a first width;

(g) forming bit line contact holes through which the top surfaces of the second cell pads are exposed, by partially etching the etch stopper between the oxide layer patterns and the second oxide layer, and concurrently, etching upper parts of sidewalls of the oxide layer patterns on both sides of the bit line contact holes so that the oxide layer patterns have portions having a second width narrower than the first width;

(h) forming bit line contact plugs by filling the bit line contact holes with a first conductive material, forming damascene bit lines on the bit line contact plugs by filling lower parts of spaces between the oxide layer patterns with the first conductive material, and etching the oxide layer patterns over the bit lines so that only the portions of the oxide layer patterns having the first width protrude above the bit lines;

(i) covering the bit lines with a mask layer and planarizing the mask layer until the top surfaces of the oxide layer patterns remaining after (h) are exposed;

(j) selectively removing the remaining oxide layer patterns, the etch stopper under the remaining oxide layer patterns, and the second oxide layer with respect to the mask layer, thereby forming storage node contact holes; and

(k) forming storage node contact plugs by filling the storage node contact holes with a second conductive material.

10. The method of claim 9, wherein (h) comprises:

depositing the first conductive material to fill the bit line contact holes and spaces between the oxide layer patterns; and

forming the bit lines by recessing the first conductive material from the oxide layer patterns, and concurrently performing an etch-back process on the resultant structure on

which the first conductive material is deposited so that only the portions of the oxide layer patterns having the first width protrude above the bit lines.

11. The method of claim 9, wherein (h) comprises:
depositing the first conductive material to fill the bit line contact holes and spaces between the oxide layer patterns;
forming the bit lines by recessing the first conductive material from the oxide layer patterns, and concurrently performing an etch-back process on the resultant structure on which the first conductive material is deposited so that the overall width of the oxide layer patterns protruding above the bit lines is reduced; and
etching the oxide layer patterns having a reduced width so that only the portions of the oxide layer patterns having the first width protrude above the bit lines.
12. The method of claim 11, wherein etching the oxide layer patterns having a reduced width is performed using dry etching, wet etching, or plasma etching.
13. The method of claim 9, wherein the mask layer is formed of a material having an etch selectivity with respect to those of the third oxide layer and the second oxide layer.
14. The method of claim 13, wherein the mask layer is formed of a nitride layer or an oxynitride layer.
15. The method of claim 9, wherein planarizing the mask layer is performed using an etch-back or a chemical mechanical polishing (CMP) process.
16. The method of claim 9, wherein the thickness of the third oxide layer is about 500 to about 6000 Å.
17. The method of claim 9, wherein the thickness of the etch stopper is about 10 to about 500 Å.